THE UNIVERSITY OF TEXAS AT DALLAS

EECT 6378 Power Management Circuits (Fall 2015)

Design of Low Dropout Regulator for Portable Application

Final Project Report

Group A

Submitted by

Rithesh Sarathy Ravikumar

Divya Siva Ranjani Sivasubramaniam

Itisha Tiwari

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**Objective:**The aim of the project is to design and implement an LDO in TSMC 0.35µm CMOS process with the given specification and examine its behavior.

|  |  |
| --- | --- |
| **Parameters** | **Specifications** |
| Minimum Supply Voltage | ≤ 1.8 V |
| Maximum output Current | ≥ 100 mA |
| Dropout Voltage | ≤ 0.2 V |
| Quiescent Current | ≤ 40 µA |
| Output Capacitor | ≤ 2 µF |
| Equivalent Series Resistance (ESR) | ≤ 2 Ω |
| Minimum loop gain amplitude | ≥ 50 dB |
| Maximum undershoots and overshoots | ≤ 100 mV |
| Transient recovery time (load step from 0 to 100 mA and the slew rate is 100 mA/10 nS | ≤ 5µS |

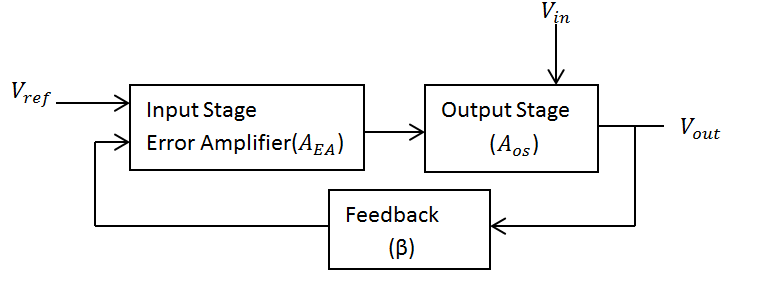
**Abstract**A low drop-out regulator has been designed with an error amplifier with a maximum overshoots and undershoots of ≤ 100 mV in 0.35 µm technology. The minimum supply voltage given is 1.8 V, and the maximum output current obtained is greater than 100 mA with an output capacitor of 2 µF. The dropout voltage is determined to be less than 0.2V.

Table 1: Given Specifications

**Introduction**  
Low Drop-out regulator is a configuration capable of maintaining desired output voltage and its applications include laptops, mobile phones, Personal Data Assistant (PDA), and pagers. The performance requirements of the regulator to ensure better stability include low quiescent current flow, low supply voltage, low output resistance, increased Phase Margin (PM), better transient response, improved noise response, minimum output voltage variation, high load current, and stability at all loads.

In this project, a single stage error amplifier and a PMOS pass transistor has been used to give a better output voltage and enhance the efficiency of the model. A pole-zero cancellation technique has been employed by using an ESR of less than 2 Ω with the output capacitor to ensure stability which generates a zero to cancel the non-dominant pole generated at the output of the error amplifier.

**Basic Block Diagram**:

  
 Figure 1: Basic Block Diagram

The basic block diagram is shown in Fig. 1. The input stage consists of an error amplifier, which compares the difference between the reference voltage and the feedback output voltage. The output of the difference between the voltages is given as input to the pass transistor of the output stage with simultaneous input voltage given to it. The output stage also consists of feedback resistors, Equivalent Series Resistance, and a varying output load resistance. The output voltage is sent as feedback to the negative terminal of the error amplifier. The output voltage is determined from the formula:  
 = + = + 🡪 (1)

**Schematic:**

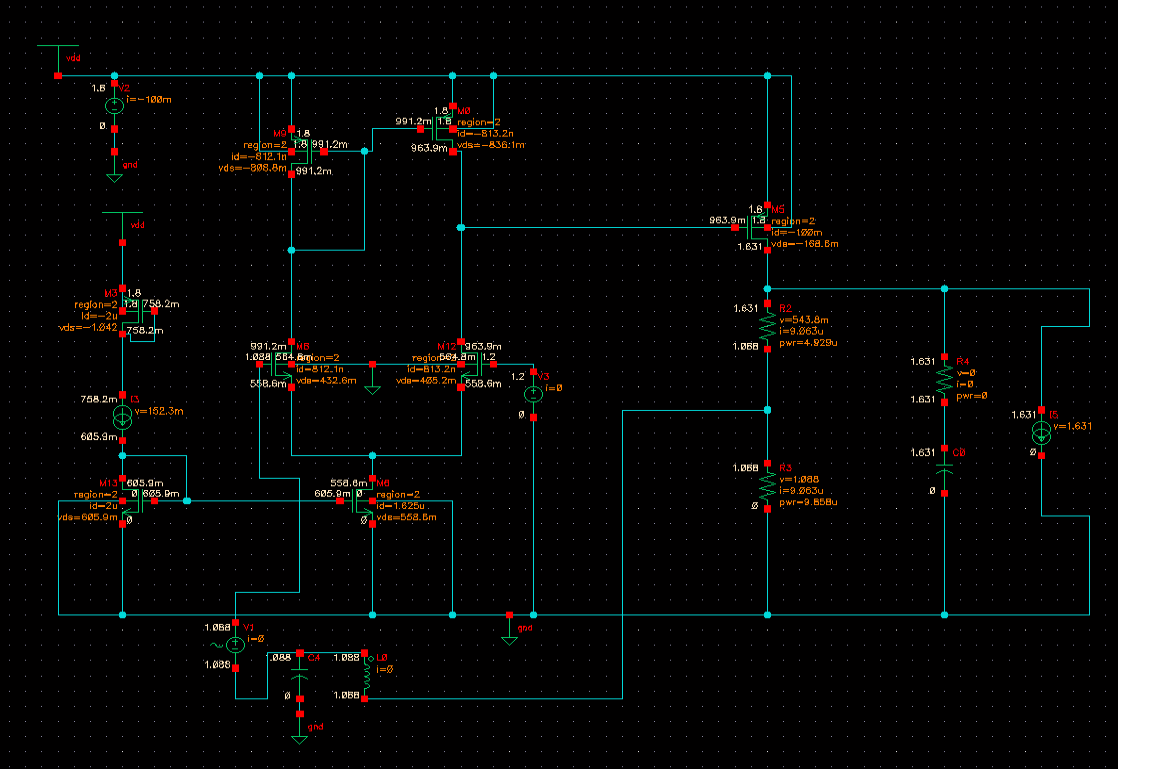
   
  
  
The schematic of the Low Drop-out Regulator is shown in Figure 2. A normal current source is used to bias the current mirror, which in turn biases the error amplifier. A voltage of 1.2 V is given as reference to one side of the amplifier, and a feedback output voltage is given to the other terminal. PMOS transistor is used as the pass device.

Figure 2: Schematic of Low Drop-out Regulator

The output phase has equivalent series resistance for pole-zero compensation.

|  |  |
| --- | --- |
| Equivalent Series Resistance | 1 Ω |
| Output Capacitor (C0) | 2 µF |
| Load | 100 mA |

Table 2: Output Phase Components specifications

**Design Procedure**

**A. Device Sizing:**

The sizing of the transistors is shown in Table 3.

|  |  |  |  |
| --- | --- | --- | --- |
| Transistor | W (m) | L (m) | Drain Current (A) |
| M3, M13 | 450 n | 450 n | 2 µ |
| M6 | 2.5 µ | 1 µ | 1.625 µ |
| M8, | 6.28 µ | 2 µ | 812.1 n |
| M9 | 4 µ | 2 µ | 813.2 n |
| M0 | 4 µ | 2 µ | 812.1 n |
| M12 | 6.28 µ | 2 µ | 813.2 n |
| M5 | 80 m | 488 n | 100 m |

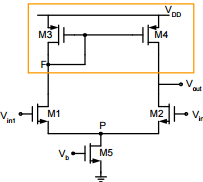
Table 3: Device Sizing

The current mirror is first designed by providing a normal current source to the mirroring circuit. The current source given is 2 µA. The sizing of the transistors can be calculated from the equation:   
  
[] = 2 🡪 (2) The calculated value is 163934.42. Keeping L as constant with the value 488 nm, the Width value is set as 80 mm.

**B. Error Amplifier**

The error amplifier consists of four transistors M8, M12, M0, and M9. The error amplifier is biased from the current mirror. A reference voltage of 1.2 V is given to one side of the amplifier and the output feedback, which is 1800 is given to the other end. The device sizing for each and every transistor can be calculated from equation (2), and the calculated values are shown in Table 2. The structure of the error amplifier is shown below. M8, M12 contain the NMOS transistors, and M0 & M9 contain the PMOS transistors. The basic circuit diagram of a normal error amplifier is shown in Figure 3.

Active Current Mirror Load

  
 Figure 3: Error Amplifier

**C. Pass Transistor**

The pass transistor is the most important component of the Low Drop-out Regulator. PMOS is used as the pass transistor because it improves the stability of the system, and also increases the overall efficiency of the system. The sizing of the pass transistor is Table 2.

**Analysis**

**A. DC Analysis**

In DC Operating point, all the transistors are designed to be in saturation with the calculated aspect ratios. The DC analysis of voltage across varying resistance was swept from 0 to 200 Ω. After analyzing DC voltage graph, we can see that the system gets stabilized at 1.621 V. So, the drop-out voltage is the difference between the input voltage and the output voltage, which is 1.8 – 1.621 that gives 0.179 V, which is less than the drop-out voltage specified. The stabilization of voltage is shown in Figure 5. Moreover, the quiescent current is also 9.903 µA.

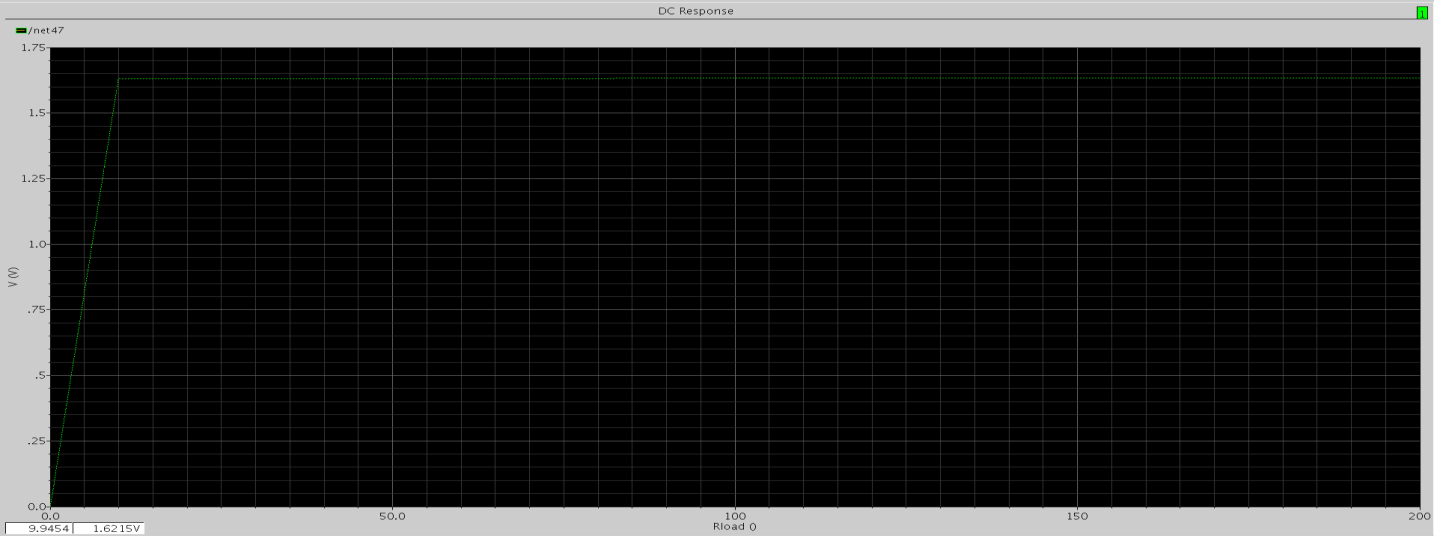


Figure 4: Output voltage Vs Varying Resistive Load

**B. AC Analysis**

Now the output resistance is replaced by a varying current source load. An inductor and a capacitor in the range of TH and TF respectively, are connected to the feedback network, and a sinusoidal voltage source is connected to the other side of the error amplifier. AC analysis has been processed, and the loop gain magnitude & Phase Margin are analyzed for different loads. The current load is varied from 0 mA to 100 mA. The analysis for different loads is illustrated in Figures 5, 6 & 7.

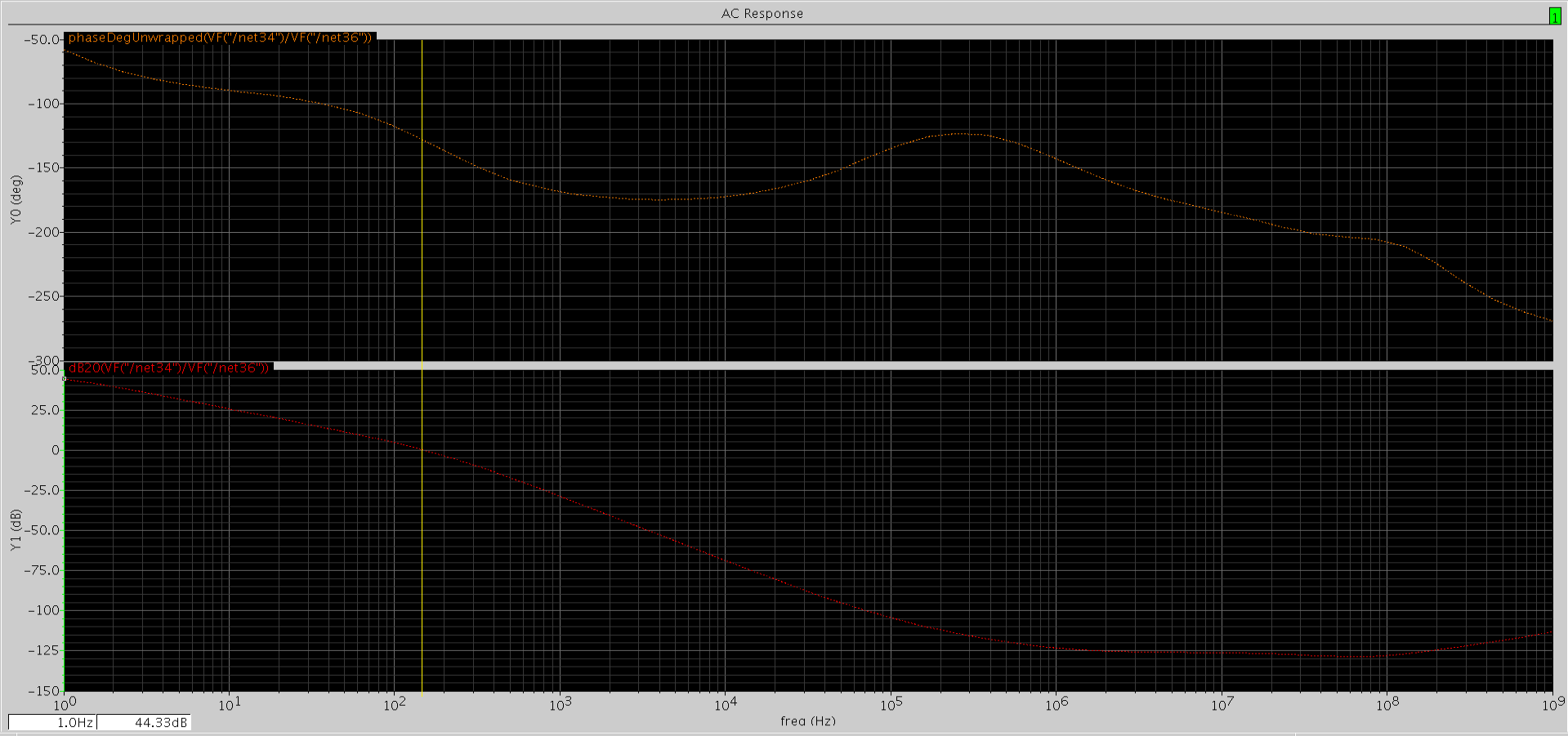


Figure 5: No Load Condition

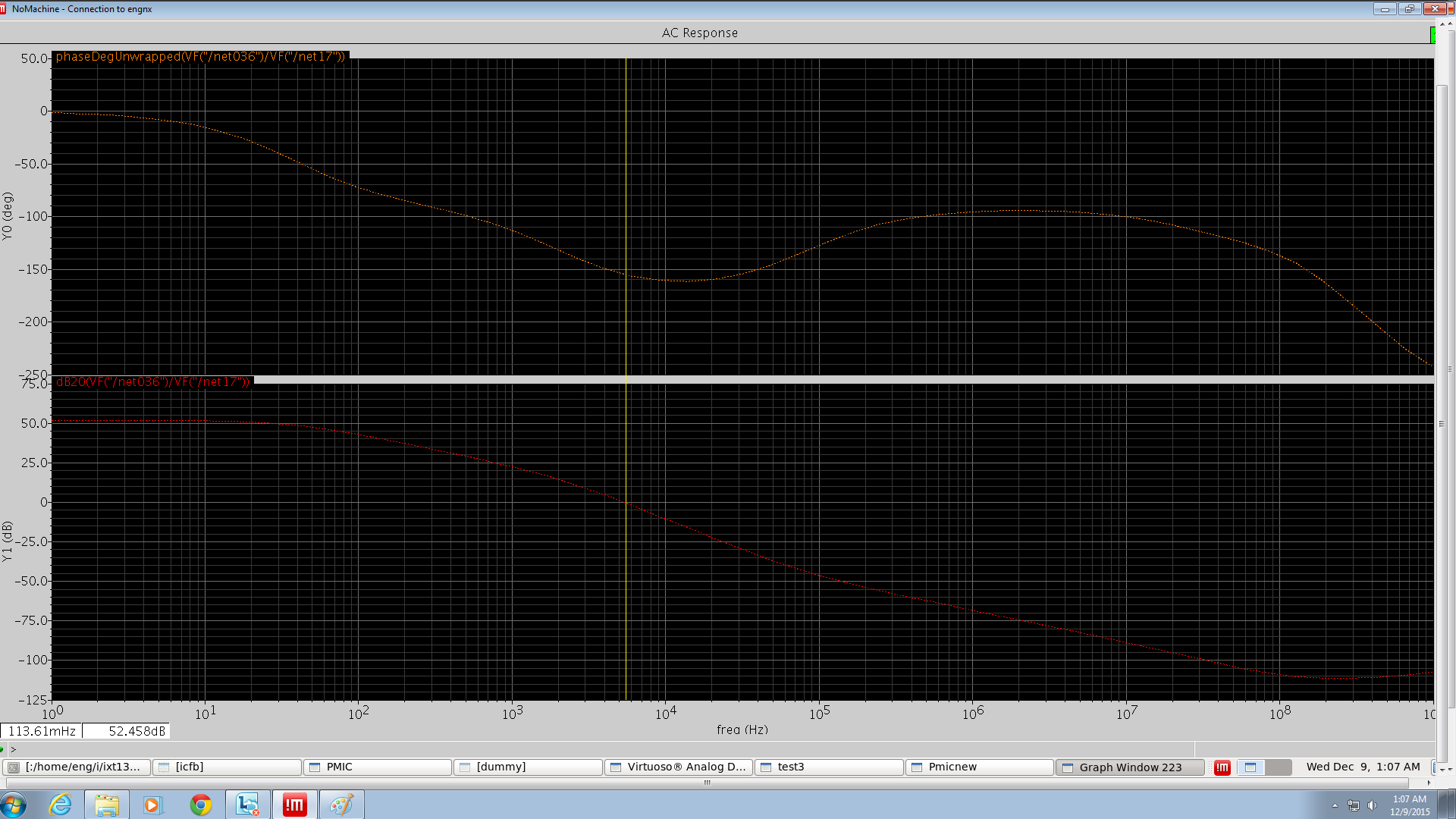


Figure 6: Mid Load Condition

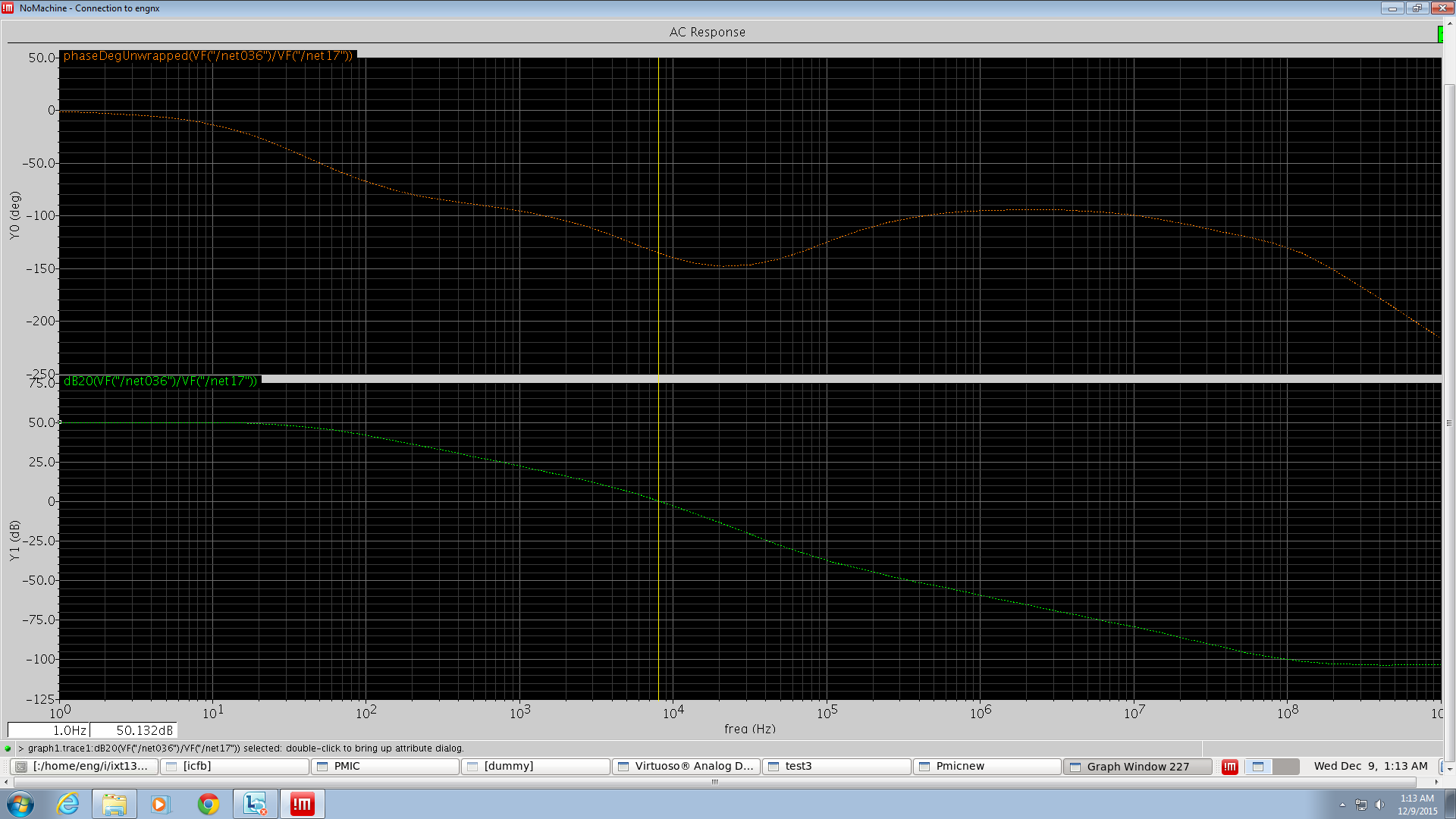


Figure 7: Full Load Condition

We can see from the plots that the loop gain magnitude for each and every load turns out to be above 50 dB, hence satisfying the specification given in the problem. Also, the Phase Margin is also above 450, ensuring stability.

**C. Transient Analysis:**

The DC current load is now replaced by a current pulse load to analyze the transient analysis to evaluate the transient recovery time, maximum overshoots, and undershoots. Step changes are given from 0 mA to 100 mA and the transient output voltage is analyzed.

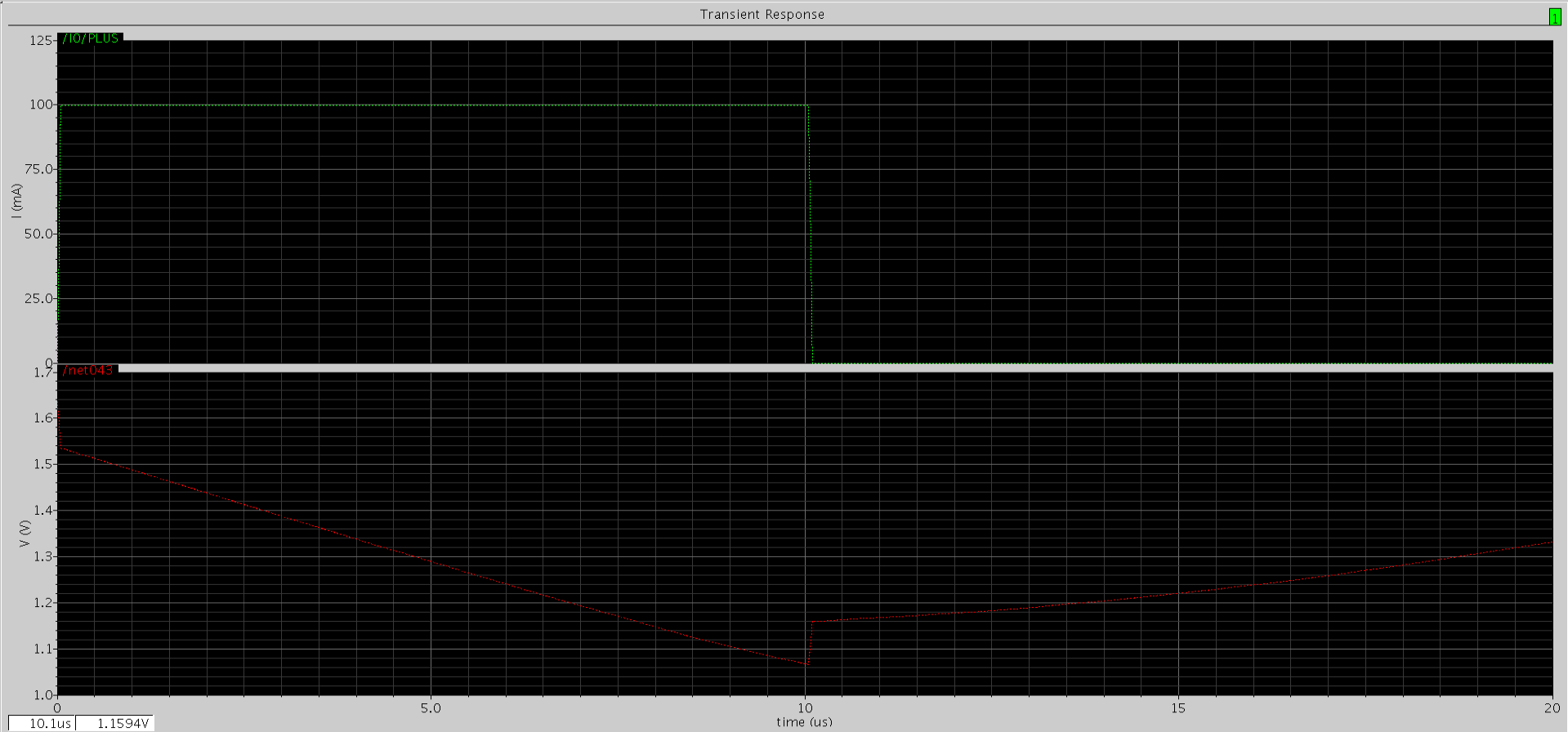
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Figure 8: Load Transient Response

The load transient response of the LDO is poor because it does not seem to settle at one point. This is because of the implementation of normal Single Stage error amplifier.

**Performance Summary of LDO**

The final results of the LDO are tabulated below:

|  |  |
| --- | --- |
| **Parameters** | **Obtained Values** |
| Minimum Input Supply Voltage | 2 V |
| Maximum output Current | 100 mA |
| Drop-out Voltage | 0.179 V |
| Quiescent Current | 9.903 µA |
| Output Capacitor | 2 µF |
| Equivalent Series Resistance | 1 Ω |
| Minimum Loop Gain Magnitude | 52.45 dB |
| Phase Margin | 46.340 |
| Maximum Overshoot | 1.6 V |
| Maximum Undershoot | 1.1 V |

Table 4: Performance Values

**Conclusion**The above simulation shows that the design LDO has a better gain and phase margin, with a maximum quiescent current obtained at 100 mA. The quiescent current has a very near constant value with respect to the load current. The only things that can contribute to the quiescent current for the MOS transistor are the error amplifier and the sampling resistor. Equivalent Series Resistance (ESR) is also implemented for Pole Zero cancellation. The transient undershoots and overshoots are poor.

In order to improve the LDO performance, a buffer circuit can be incorporated between the output of the error amplifier and the pass transistor to push the non-dominant pole to higher frequency, and also improves the transient undershoots and overshoots of the LDO.

**References**

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